

1 CLAIMS

2 1. An apparatus comprising:

3 a clock generator configured to generate a first clock signal and a second
4 clock signal, wherein the timing relationship between the first and second clock
5 signals is arbitrary and wherein the first and second clock signals are individually
6 adjustable; and

7 a phase detector coupled to receive the first and second clock signals, the
8 phase detector generating a skip signal by integrating the first clock signal,
9 wherein the skip signal indicates whether the first clock signal is ahead of the
10 second clock signal.

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12 2. An apparatus as recited in claim 1 wherein the value of the skip
13 signal is based on the phase difference between the first clock signal and the
14 second clock signal.

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16 3. An apparatus as recited in claim 1 wherein the skip signal has a first
17 value if the first clock signal is ahead of the second clock signal and the skip
18 signal has a second value if the second clock signal is ahead of the first clock
19 signal.

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21 4. An apparatus as recited in claim 1 wherein the phase detector
22 generates a skip signal by integrating the first clock signal over one half of a clock
23 cycle.
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1 5. An apparatus as recited in claim 1 further including an inverter
2 coupled to an output of the phase detector.

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4 6. An apparatus as recited in claim 1 wherein the phase detector is a
5 quadrature phase detector.

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7 7. An apparatus as recited in claim 1 wherein the first and second clock
8 signals are calibrated individually.

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10 8. An apparatus as recited in claim 1 wherein the skip signal indicates
11 whether a load pulse should be sampled.

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13 9. A method comprising:
14 receiving a first clock signal and a second clock signal;
15 shifting the phase of the first clock signal by 90 degrees using a quadrature
16 phase detector; and
17 generating a skip signal indicating whether a load pulse should be sampled,
18 wherein the value of the skip signal is based on the phase difference between the
19 first clock and the second clock.

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21 10. A method as recited in claim 9 wherein the skip signal has a first
22 value if the first clock signal is ahead of the second clock signal and the skip
23 signal has a second value if the second clock signal is ahead of the first clock
24 signal.

1 **11.** A method as recited in claim 9 wherein the shifting the phase of the
2 first clock by 90 degrees includes integrating the first clock signal.

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4 **12.** A method as recited in claim 9 wherein the shifting the phase of the
5 first clock by 90 degrees includes integrating the first clock signal over one half of
6 a clock cycle.

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8 **13.** A method as recited in claim 9 wherein the first and second clock
9 signals are individually adjustable.

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11 **14.** A memory system comprising:
12 a memory storage device;
13 a data bus coupled to the memory storage device;
14 a clock generator configured to generate a first clock signal and a second
15 clock signal, wherein the timing relationship between the first and second clock
16 signals is arbitrary; and
17 a memory controller coupled to the data bus, the memory controller
18 including a phase detector coupled to receive the first and second clock signals,
19 the phase detector generating a skip signal based on the phase difference between
20 the first clock signal and the second clock signal.

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22 **15.** A memory system as recited in claim 14 wherein the phase detector
23 generates a skip signal by integrating the first clock signal over one half of a clock
24 cycle.

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1 **16.** A memory system as recited in claim 14 wherein the first and
2 second clocks are individually adjustable.

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4 **17.** A memory system as recited in claim 14 wherein the phase detector
5 is a quadrature phase detector.

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7 **18.** A memory system as recited in claim 14 wherein the first and
8 second clock signals are calibrated individually.

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10 **19.** A memory system as recited in claim 14 wherein the skip signal
11 indicates whether the load pulse should be sampled.

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13 **20.** A memory system as recited in claim 14 wherein the skip signal has
14 a first value if the first clock signal is ahead of the second clock signal, and the
15 skip signal has a second value if the second clock signal is ahead of the first clock
16 signal.